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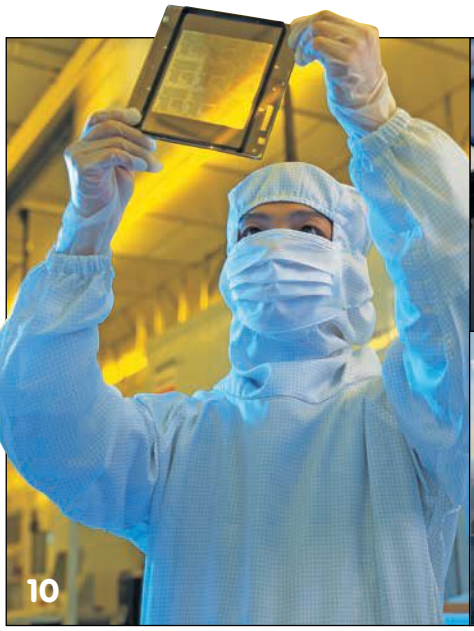

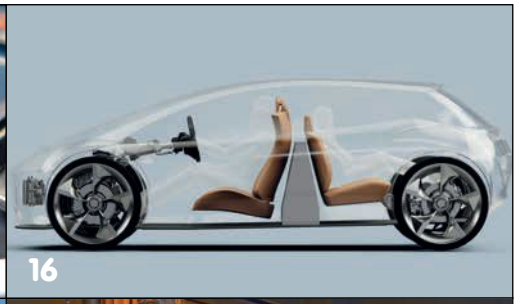

COVER IMAGE: Taiwan Semiconductor Manufacturing Co., Ltd.

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A new network contender

WILL VODAFONE'S DECISION TO USE SAMSUNG TO SUPPLY ITS 5G NETWORK EQUIPMENT HELP BREAK-UP THE 'COSY' DUOPOLY OF NOKIA AND ERICSSON?

Earlier this month the British telecoms group Vodafone unveiled its strategic O-RAN vendors, a list that included the likes of Dell, NEC, Samsung Electronics, Wind River, Capgemini Engineering and Keysight Technologies. According to Vodafone its initial focus will be on 2,500 sites in the UK, in what will be one of the largest O-RAN deployments in the world, as it looks to extend 4G and 5G coverage across the UK.

But it was the news that Vodafone had chosen Samsung Electronics to supply its 5G network equipment that was probably the most important aspect of the announcement.

Last year the UK announced that it would be requiring Huawei to remove all equipment from its 5G network by the end of 2027, citing national security risks, which raised questions over the roll-out and cost of delivering 5G.

The network equipment market has traditionally been dominated by Nokia, Ericsson and Huawei, and ever since the mobile operators were told they were going to have to phase out Huawei's equipment they've been faced by what appeared to be an even more limited choice for their 5G equipment.

Another consequence of banning Huawei was that a growing number of telecom operators started looking at deploying O-RAN, a wireless network architecture which allows mobile operators to essentially 'mix and match' equipment from various suppliers providing much greater flexibility.

Johan Wibergh, Vodafone's chief technology officer, said that by using O-RAN the company would be able to release new features simultaneously across multiple sites, add capacity more quickly and resolve outages "instantly".

That trend seems to be paying off for Samsung which is gaining market share as European mobile operators like Telefonica and Orange hold talks with the firm.

Samsung has a very strong 5G RAN portfolio that covers mobile broadband, fixed wireless access and private 5G networks and, as a consequence, is now being seen as a 'real' contender in this fast growing and extremely important market.

Prior to Vodafone's decision Samsung had already won a $6 billion deal with Verizon in the US, and analysts are now calling the announcement by Vodafone a "breakthrough" for Samsung.

Vodafone's decision is being described as a key moment for 5G in the UK but it should also be seen as one for Samsung, which until recently had been considered out of the game and an also-ran against Nokia and Ericsson.

Having successfully broken up this duopoly it would appear that plenty of other deals are likely to follow.

Neil Tyler, Editor (neil.tyler@markallengroup.com)

"Having successfully broken up the Nokia/Ericsson duopoly it would appear that plenty of other deals are likely to follow for Samsung."

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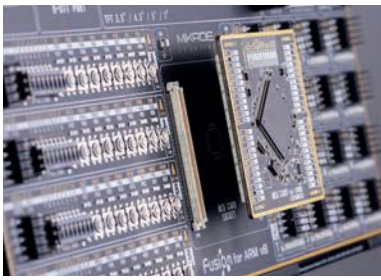
New SiBRAIN MCU development standard

SIBRAIN MCU DEVELOPMENT STANDARD A 'GAME-CHANGER' FOR EMBEDDED SYSTEMS DESIGN. **NEIL TYLER** REPORTS



MikroElektronika (MIKROE) has launched SiBRAIN, a new standard for add-on development boards that simplifies the installation and exchanging of a microcontroller (MCU) on a development board equipped with the SiBRAIN socket. SiBRAIN enables embedded designers to try out different MCUs in a prototype system without having to invest in expensive hardware or learn new tools. It currently support MCUs from: Microchip, ST, NXP and Texas Instruments.

SiBRAIN uses the same 'plug & play' concept which underpins MIKROE's Click board product range.

Depending on the MCU type, its pin count, and the number of required external components, there are different SiBRAIN add-on boards, each is a self-contained unit, allowing the development system to operate on a logic level, without having to facilitate the specific requirements of many different MCUs. Designers can swap SiBRAIN MCU cards easily during the development phase, without any additional hardware.

Each card is equipped with two high-speed 168-pin mezzanine connectors with the standard SiBRAIN socket pin-out. Cards can be installed on any development board with the SiBRAIN socket, and the design eliminates incorrect orientation and placement. MIKROE offers more than 100 SiBRAIN boards covering popular MCUs such as STM32, PIC32, TIVA, MSP432 Kinetis with new cards added on a weekly basis.

Commenting Nebojsa Matic, CEO of MIKROE, said, "The SiBRAIN card and socket standard is a game-changer, saving months of wasted development time and money and providing enormous design flexibility."

Shared design data for cooling simulation

Siemens Digital Industries Software has announced the establishment of JEP181 - a neutral file, XML-based standard from the JEDEC Solid State Technology Association, a standards body for the microelectronics industry.

JEP181 looks to simplify thermal model data sharing between suppliers and end-users in a single file format called ECXML (Electronics Cooling eXtensible Markup Language).

The new standard was created to address a significant challenge for electronics manufacturers: as increasingly powerful processors allow companies to pack more performance and functionality into their designs, the effective management of heat dissipation and other thermal factors has become essential to the successful design of their next-generation electronics products.

While advanced electronics cooling simulation technologies enable the creation of highly accurate thermal models of new product designs, the absence of a uniform format for the exchange of thermal simulation data throughout supply chains has created duplication of effort and the potential introduction of errors into the stream.

Proposed via the JEDEC JC15 committee, the JEDEC JEP181 standard simplifies thermal model data sharing and will help electronics manufacturers reduce the time required to simulate and validate their thermal models.

Commenting Ghislain Kaiser, senior director, Intel, said, "This standardised format will allow more interoperability between engineering teams, leading to substantial time and cost savings by removing design barriers previously common in thermal engineering."

"As a leader in industrial software solutions, our contribution to the new JEP181 standard can help drive the digitalization of design data to reduce both time and errors for today's innovative electronics products," said Jean-Claude Ercolanelli senior VP of Simulation and Test Solutions, Siemens Digital Industries Software. "Enabling a seamless digitalized software flow can radically increase the efficiency and accuracy of thermal simulation and enhance the performance and reliability of digital twin prototypes and manufactured products."

CPI joins battery project

CPI JOINS THE ALBATROSS PROJECT TO ENHANCE NEXT-GENERATION EV BATTERY PACKS. **NEIL TYLER** REPORTS

CPI, the technology innovation centre and a founding member of the High Value Manufacturing Catapult, is joining the Advanced Light-weight BATteRy systems Optimised for fast charging, Safety, and Second-life applications (ALBATROSS) project.

Electric vehicles (EVs) have an increasingly important role in meeting climate targets worldwide; but issues around battery durability, lifespan and charging times have slowed widespread adoption.

The ALBATROSS project is developing advanced battery pack designs for EVs that could help boost sales, significantly reduce carbon emissions and give European vehicle manufacturers a commercial advantage.

ALBATROSS represents a pan-European EU consortium, coordinated by Yesilova Holding, with twenty-one partners. Work commenced at the beginning of 2021 and will continue until December 2024. EU Horizon 2020 is providing €9.9 million in funding.

Central to this project is the reengineering of a BMW i3 all-electric vehicle battery pack. The goal is to improve its current capacity and driving range by replacing a Lithium-Manganese battery with cells containing a Nickel-Manganese-Cobalt blend. This will help to achieve a Peak Energy Density of >200Wh/kg and prolong battery lifespan. In addition to a 20% weight reduction, the new design will increase surface area to enhance cooling.

Combined with innovative thermal management and sensor technologies, the novel battery pack would enable a rapid charging time of only 30 minutes.

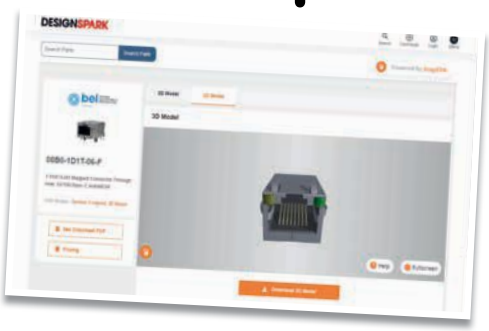
While the initial design is based on improvements to the battery pack of a BMW i3, ALBATROSS intends to deliver battery packs that can be applied to delivery vans, buses and heavy-duty vehicles. Another objective is to develop sustainable end-of-life solutions and processes allowing battery pack components to be repurposed or recycled safely.

CPI's expertise in printed electronics and sensors, electronic materials and roll to roll processing is seen as having a crucial role within the project. CPI will be working in close collaboration with PST Sensors Europe, a UK-based high-tech SME specialising in thermal sensors and heaters. Together, they will jointly lead the development of printed sensors and heaters combined with hybrid electronic assemblies to enhance battery performance and temperature control. CPI will also be involved in integrating, demonstrating and testing the ALBATROSS battery pack at a module level.

Dave Barwick, Technology Manager at CPI, said, "This project is an exciting opportunity for CPI to further develop and utilise its capabilities in the energy storage space as well as contributing to the optimisation of EV batteries to support the drive towards net zero."

DesignSpark integrates SnapEDA

SNAPEDA AND DESIGNSPARK ANNOUNCE A NEW COLLABORATION TO HELP ENGINEERS DESIGN FASTER. **NEIL TYLER** REPORTS



SnapEDA, the search engine for electronics design, and DesignSpark, an online design community and resource centre for design engineers, have announced a new collaboration that's intended to help engineers design faster, regardless of which PCB design tool they use.

The collaboration will augment the DesignSpark website with the SnapEDA search engine, allowing engineers to discover and design-in millions of electronic components through free computer-aided design (CAD) models that are compatible with nearly all major PCB design tools.

With over a billion electronic components in production, part selection and design-in are significant bottlenecks when designing electronics. In addition to the sheer volume of parts to choose from, engineers need to be able to procure sophisticated digital models for each component in their designs. This prerequisite for complex design content is a burden on engineers that can hamper innovation.

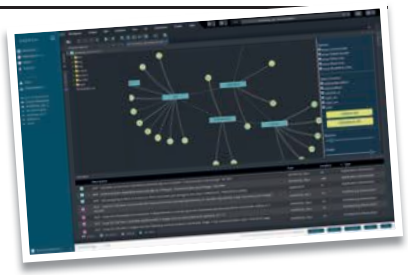
The new SnapEDA search function on the DesignSpark website is intended to make it easier for engineers to search and design-in electronic components, allowing engineers to jump straight to design. Engineers can search for a keyword like 'Bluetooth' or 'usb type c' to discover new components, or enter a specific part number. Once they've selected a product, they can download the CAD model instantly.

"Since launching DesignSpark, RS Components has demonstrated its commitment to supporting the engineering community through tools and resources," said Natasha Baker, Founder and CEO of SnapEDA. "This commitment resonates with us here at SnapEDA, where we have similarly been committed to helping engineers design faster with free, innovative design tools and resources we've brought to the market."

Powered by SnapEDA's own patented verification technology, the new integration also includes datasheets and other specifications provided by RS Components, as well as the ability to check prices and purchase components.

Supported PCB design formats include DesignSpark PCB, Altium, KiCad, Fusion360, Cadence Allegro, OrCAD, EAGLE, Pulsonix, DipTrace, Proteus, ExpressPCB Plus, CircuitStudio, PADS, PCB123, Target 3001!, and P-CAD.

Xilinx acquires Silexica



Xilinx has announced that it has acquired Silexica, a privately-held provider of C/C++ programming and analysis tools.

Silexica's SLX FPGA tool suite supports developers building applications on FPGAs and Adaptive SoCs. The company's technology will be integrated with the Xilinx Vitis unified software platform and will help to substantially reduce the learning curve for software developers building sophisticated applications on Xilinx technology.

Leveraging standard high-level synthesis tools from Xilinx, the SLX FPGA tool suite tackles non-synthesizable and non-hardware aware C/C++ code, detects application parallelism, inserts pragmas, and determines optimal software and hardware partitioning. This enables designing at a higher level of abstraction, orders of magnitude faster simulation, and a better result through high-level optimisations and design space exploration.

"Software programmability is imperative to our long-term goal to accelerate the path from software to application-optimised hardware systems," explained Salil Raje, executive vice president and general manager, Data Center Group, Xilinx. "Silexica's technology complements our existing Vitis solution and roadmap and will accelerate our ability to attract a wider range of developers seeking to leverage our heterogeneous computing architectures."

Silexica was spun out of RWTH Aachen University in 2014 and it is headquartered in Cologne, Germany, with additional offices in Silicon Valley and Japan. It serves companies in the automotive, robotics, wireless communications, aerospace, and financial industries and has received $28 million in funding from international investors.

Testing 3D magnetic sensors

Hprobe, a provider of semiconductor Automated Test Equipment (ATE) for magnetic devices, has demonstrated a new 3D magnetic generator design resulting in magnetic field accuracy of less than 5µT (5 microteslas) for wafer level probing of 3D angular magnetic sensors.

Operating with automated wafer probing stations and external electrical testers, this is being described by the company as a 'major breakthrough'. offering significant throughput performance for testing advanced 3D magnetometers.

The system provides both high flexibility and compatibility with existing end-user platforms and high-volume manufacturing requirements. It is the latest evolution in Hprobe's patented 3D magnetic field generator technology for single and multi-site testing at wafer level, under a magnetic field.

"With this new achievement, we enable the implementation of new test strategies to improve test efficiency, allowing validation of more accurate sensor products," explained Siamak Salimy, CTO and co-founder of Hprobe.

Advanced magnetic sensors are used for various automotive, consumer and industrial applications to extract positioning, angular, strength and direction information. They sense physical parameters using a magnetic field and transmit electrical responses for further processing. To validate these sensors for end applications they have to be tested under extremely demanding and accurate 3D magnetic fields.

Self-testing in Embedded Systems

Unless available memory is totally exhausted, in an embedded design it is worthwhile considering the implementation of some self-testing capabilities.

Modern electronics tends to be amazingly reliable, but failures are still possible. In an embedded system there are broadly four categories of failure:

- CPU
- Peripheral
- Memory
- Software errors

If a CPU fails, it tends to be a hard failure. This does not offer any possibility for self-testing. Partial failure of a CPU is very unlikely. In a multicore system, it is good practice to assign one of the cores as "master" so that it can monitor system integrity.

Peripherals can fail in various ways, but many modes of failure are very device/application specific. If a device fails to respond to its address, the trap occurs; it is essential to include a trap handler to process this fault. Otherwise, communications devices commonly include a "loopback" mode that enables testing of transmission and reception and associated interrupts.

Memory failure is always a possibility. This failure may be transient – i.e., a single bit being flipped by a passing cosmic ray. It is generally not possible to detect such a fault and it may cause a software crash. It is, therefore, essential to accommodate crash recovery. A hard failure maybe a lack of address response or bits stuck at 0 or 1. A trap handler deals with the former, but the latter requires some specific testing. Comprehensive memory testing can only be done on device start-up. A *Moving Ones* test is effective.

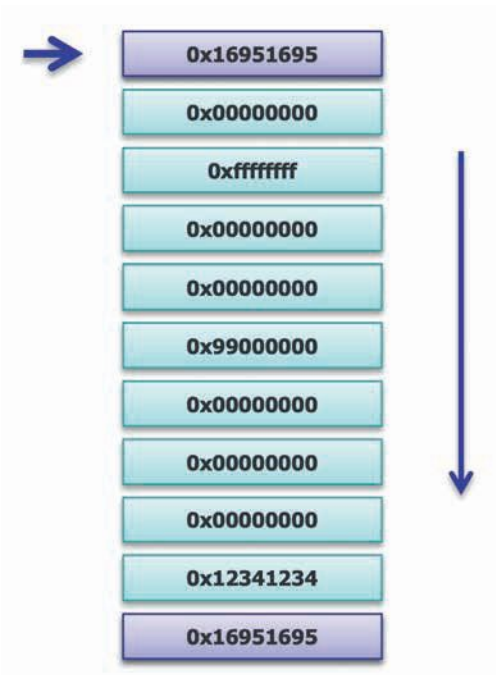
```
set every bit of memory to 0
for each bit of memory
{
   verify that all bits are 0
   set the bit under test to 1
   verify that it is 1
   verify all other bits are 0
   set the bit under test to 0
}
```

Moving Ones Test

While the device is operating, pattern testing can be performed on individual bytes/words, which may highlight certain types of failure.

The most complex part of modern devices is software. Although software does not exactly wear out, its complexity can result in faults that are difficult to detect during development. Good, defensive coding techniques can help anticipate some problems. Broadly, there are two types of software error: data corruption and code looping.

Data corruption can be caused by pointer misusage, which is hard to detect or prevent, but it can also be as a result overflow of a data structure, like an array or the stack. The insertion of "guard words" can assist with the detection of overflow before any damage is caused.



Stack Guard Words

Code looping can be addressed by careful design – precautions like timeouts on waiting for devices – or some kind of watchdog facility (in hardware or software) that traps unresponsive code.

Colin Walls, Siemens Embedded

MASTER OF THE UNIVERSE

This year's Technology Symposium highlighted TSMC's dominance of the semiconductor market and, considering its investment plans, that's likely to continue for some time. By **Neil Tyler**

Earlier this month Taiwan Semiconductor Manufacturing Company (TSMC) used its 2021 Technology Symposium to unveil a range of new innovations in advanced logic technology, specialty technologies, advanced packaging and chip stacking technologies as well as confirming a number of significant new investments in manufacturing and research capacity around the world.

Among the new offerings were the N6RF for next-generation 5G smartphones, the N5A for state-of-the-art automotive applications and enhancements across its range of 3D Fabric technologies.

"Digitalisation is transforming society faster than ever as people use technology to overcome the barriers created by the global pandemic to connect, collaborate, and solve problems," said Dr. C.C. Wei, CEO of TSMC in his speech opening the symposium and he concluded that this new world was full of, "opportunities for the semiconductor industry."

Founded in 1987, TSMC is the world's largest contract chipmaker and pioneered the pure-play foundry business model. In 2020 it deployed 281 distinct process technologies and manufactured 11,600 products for over 500 customers. As a consequence, it's currently Asia's most valuable manufacturing company with a market capitalisation in excess of $560 billion.

TSMC's success has been built on developing and deploying cutting edge technologies and it was the first foundry to provide 5-nanometer production capabilities and is currently building a plant to make 3-nanometer chips, which are expected to be up to 70 per cent faster and more power-efficient than the most advanced chips currently available.

According to C.C. Wei the company's 3-nanometer chip-making technology is on track and volume production at the company's "Fab 18" factory in Tainan, Taiwan, is scheduled to start in the second half of 2022.

TSMC has been described as being at the 'centre of the electronics universe' and has announced a massive programme of investment in new cutting-edge technology and in manufacturing capabilities - not only in Taiwan, but in the US too.

In the US TSMC has started construction at a site in Arizona where it plans to spend $12 billion building a computer chip factory using the company's 5-nanometer production technology. Volume production is expected to start in 2024. There have also been reports that it is planning to build a further six factories at this site over a possible 10- to 15-year time period.

TSMC has also announced that it is setting up a subsidiary in Japan to conduct research into new semiconductor materials.

In April the company confirmed a $100 billion investment plan over the next three years to increase capacity at its factories – which includes $30 billion in spending this year alone.

"That will give us enough manufacturing capacity to support the growth of our clients," said Wei.

"Digitalisation is transforming society faster than ever as people use technology to overcome the barriers created by the global pandemic to connect, collaborate, and solve problems"
Dr. C.C. Wei

New innovation unveiled

At its recent symposium TSMC made a series of announcements that will be critical in supporting some of the key technologies that are driving the digital transformation Wei mentioned. These included the N4 enhancement to the company's 5nm family driving further improvements to their performance, power efficiency and transistor density, as well as a reduction of mask layers and closer compatibility in design rules with N5.

TSMC said that the N4 development had 'proceeded

Image credit: Taiwan Semiconductor Manufacturing Co., Ltd.

smoothly' since its announcement at last year's Technology Symposium, with risk production set for later this year.

TSMC also announced that it was introducing N5A, the newest member of the 5nm family. The N5A process is intended to meet the growing demand for computing power in newer and more intensive automotive applications such as AI-enabled driver assistance and the digitisation of vehicle cockpits.

TSMC's head of global marketing Godfrey Cheng, said that, "Compared to TSMC's N7 technology with the Automotive Service Package, N5A delivers a ~20% improvement in performance or a ~40% improvement in power efficiency and a ~80% improvement in logic density."

According to Cheng, the N5A brings the same technology used in supercomputers to vehicles, and will be able to deliver the performance, power efficiency and logic density of N5 while meeting the stringent quality and reliability requirements of AEC-Q100 Grade 2 as well as other automotive safety and quality standards.

With its factory under development in Taiwan, TSMC's N3 technology is set to push the envelope even further, providing the most advanced technology when it begins volume production next year.

Relying on the TSMC's FinFET transistor architecture N3 will be able to offer up to a 15% speed gain or consume up to 30% less power than N5, and provide up to a 70% logic density gain.

Turning to 5G TSMC's Yujun Li, Director High Performance Computing Business Development, said, "Smartphones are now an integral part of our lives and are helping to accelerate digital transformation and with 5G will enable many more applications. As a consequence, we are seeing very strong transistor growth in CPUs, GPUs and in newer AI accelerators."

Above: TSMC's new N6RF compared to the 16 FFCRF

5G enabled chips are integrating more functionality and components and are growing in size.

"As a result they are in competition with the battery for the limited amount of space inside the smartphone," said Li.

In response, TSMC unveiled the N6RF process which brings the benefits of the advanced N6 logic process to 5G radio frequency (RF) and WiFi 6/6e solutions.

According to Li, the N6RF transistors are able to achieve more than 16% higher performance over the prior generation of RF technology at 16nm and are able to support significant power and area reduction for 5G RF transceivers for both sub-6 gigahertz and millimeter wave spectrum bands, but do so without affecting either the device's performance or battery life.

Jerry Tzou, Director, Advanced Packaging Business Development, announced that TSMC was continuing to expand its 3D Fabric family of 3D silicon stacking and advanced packaging technologies and was now offering larger reticle-size for both its InFO_oS and CoWoS packaging solutions, enabling larger floor plans for chiplet and high-bandwidth memory integration.

In addition, the chip-on-wafer (CoW) version of TSMC-SoIC will be qualified on N7-on-N7 this year with production targeted for 2022 at a new fully-automated factory.

For mobile applications, TSMC said that it was introducing its InFO_B solution, which has been designed to integrate a powerful mobile processor in a compact package supporting mobile device makers' DRAM stacking on the package.

"These innovations in chip stacking technologies will enable customers to deliver next generation innovations and we're expanding our capabilities to support growing customer volume needs," said Tzou.

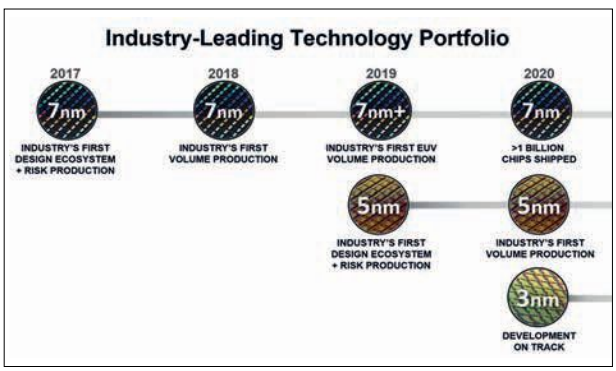
Market dominance

The scope of the announcements made, and the commitments to further investment, highlighted the dominance of TSMC in the semiconductor market. That dominance has, in turn, been brought into even sharper focus by the on-going chip shortage which has seen slowdowns and suspension of production around the world, affecting many different industries – notably the automotive sector.

Few companies are able to match TSMC in terms of its technology and manufacturing capabilities and those attempting to do so would be faced with prohibitive costs. Despite that, a number of governments, including the United States, the European Union, Japan and India are all said to be contemplating spending billions of dollars on new chip fabrication plants.

For some, there are concerns that current shortages could continue well into 2023 and that, in the longer term, semiconductor production in Asia may not always be calibrated to meet the needs of all customers.

As Victor Peng, Xilinx CEO, said to New Electronics last month, "Across the industry everyone is looking to



build more capacity and are working closely and co-operating more with their customers, including those supplying packaging and substrates. But it remains a difficult trading environment and we will have to continue to handle limitations in terms of supply."

That certainly applies to many industries and how they deal with TSMC and the broader semiconductor industry. Interviewed in the Financial Times, Ambrose Conroy, founder and chief executive of Seraph, a supply chain consultancy, warned that semiconductor manufacturers were now the "giants" and that purchasing teams – even those in the automotive industry - were little more that the "ants".

An observation which Joseph Notaro, VP of WW Automotive Strategy and Business Development at ON Semiconductor, tended to agree with. "The supply chain has turned into a really big story at the moment but when you look at the automotive supply chain, for example, it is not so much about market conditions but rather the way in which the market operates. Lean manufacturing and just-in-time are central to the way the supply chain currently works and while that's fine when it's stable and predictable, it's not so good with the level of market disruption we've been seeing."

Looking beyond the current issues around the global supply chain the dominance of Taiwan, and TSMC in particular, has added another dynamic to the on-going rivalry between the US and China – not only in terms of their growing political, military and economic rivalry but also in terms of technological leadership.

With more than two-thirds of advanced computing chips now manufactured in Taiwan there are worries that future tensions with China could have serious implications for manufacturers in the West with supplies curtailed or even cut-off.

TSMC's semiconductors are designed and sold in products used by branded vendors such as Apple, AMD or Qualcomm and it controls more than half of the world market for made-to-order chips and that dominance is only likely to grow with the rolling out of new process nodes whether that's 7nm, 5nm or 3nm.

Image credit: Taiwan Semiconductor Manufacturing Co., Ltd.

Above: Today TSMC accounts for over 90 per cent of the market for the most advanced nodes

Today TSMC accounts for around 90 per cent of the market for the most advanced nodes, so is the world too dependent on this one company?

One analyst described the situation as dangerous, "the industry is incredibly dependent on TSMC and it is quite risky."

The key issue is the cost of developing and manufacturing semiconductors. Twenty years ago there were over 20 foundries all at the cutting edge, today there's only TSMC and with the enormous costs of development and the investment that's required in new production capacity most foundries are now focused on design – leaving manufacturing almost entirely to TSMC. Even Samsung and Intel are struggling to keep up.

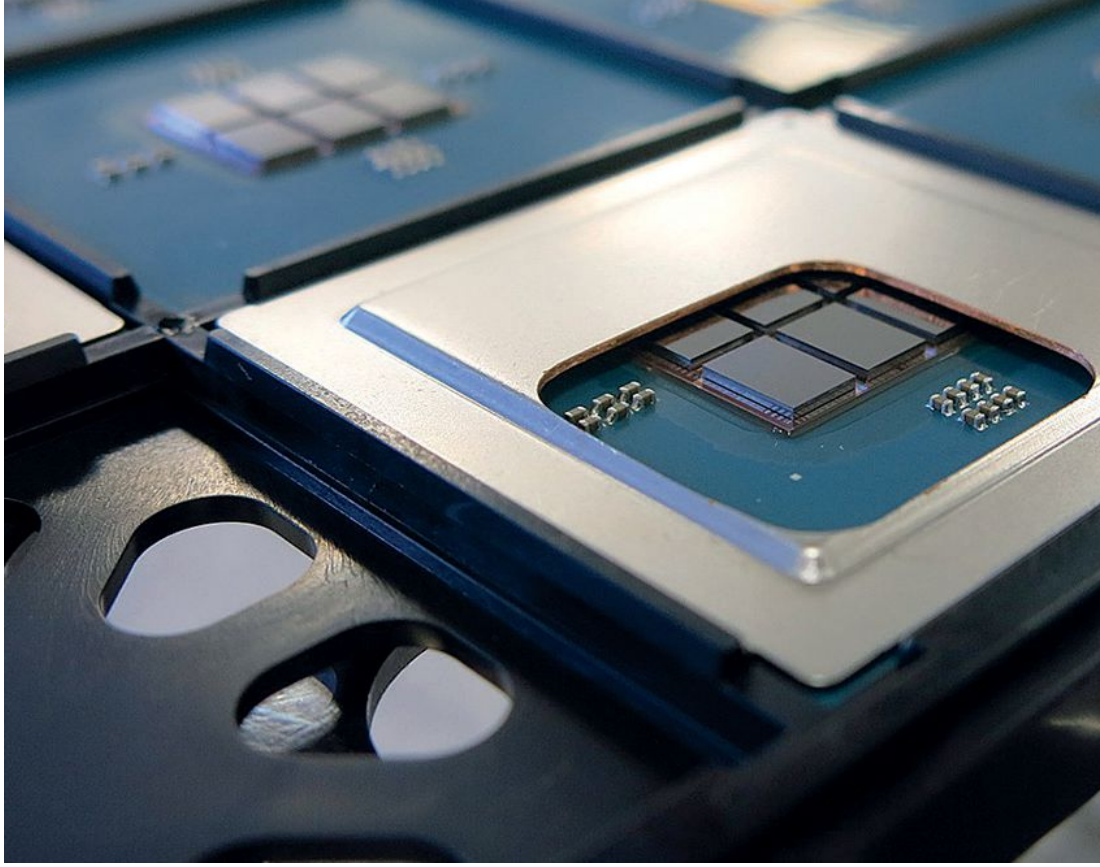
In fact Intel has outsourced production to TSMC as a result of production difficulties with its 10nm and 7nm technology nodes and has even faced calls from some investors that it should become 'fabless', a call that was rejected by the company's CEO Pat Gelsinger. Despite that analysts say that upwards of 20 per cent of Intel's CPU production is likely to be outsourced to TSMC in 2023, and TMSC is already investing around $10bn in capacity to meet that demand.

It's those kinds of figures that suggest that TSMC's position, for the time being, is unassailable.

Investment is in the billions and has to be on-going if companies are to remain at the cutting-edge and critics of proposals to invest in new capacity around the world suggest that proponents of such a strategy fail to grasp the scale and costs involved.

TSMC's commitment to huge capital investment plans suggest that it is determined to hold on to its lead. Much of the company's projected capital expenditure will go into extreme ultraviolet (EUV) lithography machines - cutting-edge fabrication units – a move that will keep it well ahead of any potential competitor.

TSMC looks unassailable and is currently set to remain very much at the centre of the semiconductor universe.



Return of the **multichip**

Chiplets are looking more attractive as silicon area spirals upwards. But none of the decisions around their use are easy. By **Chris Edwards**

One of the predictions made by Gordon Moore in 1975 during an IEDM keynote where he refined the ideas that gave rise to Moore's Law was that chips would get bigger pretty quickly and that this growth would be a major contributor to scaling. He only projected as far as 1980 but his estimates pointed to die area at least doubling in five years: hitting 60 square millimetres by that time. In the mid-2000s, Intel did its best to keep up with the extrapolation courtesy of its reticle-busting Itanium processors that clocked in at almost 700sq mm. With just a handful of customers, it was clear that most of the industry was happier with smaller devices and using more of them.

A little over a decade later, the burst in activity around artificial intelligence has put big chips back on the menu.

"Chips are getting larger and the area is mostly consumed by the AI blocks," said Mustafa Badaroglu, principal engineer at Qualcomm, in his outline of the changes to the International Roadmap for Devices and Systems (IRDS) "More Moore" section during the organisation's May preview seminar. Whereas SoCs for mobile devices might continue to opt for die sizes below 100 square millimetres, AI is taking them to 500 and beyond.

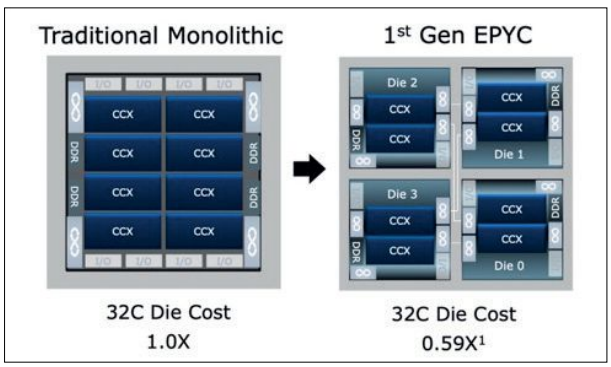
Cerebras has to some extent kept Moore's extrapolation alive with a processing array that covers almost 50,000sq mm of silicon. As the reticle area of a scanner limits how much of the wafer can be exposed at one time to less than 1000sq mm, the company worked with TSMC to find a way to easily stitch the component chips together into a larger array.

Poor yield is a major problem for many superchips, a factor that is not helped by random defect counts that are going up as processes become denser and far more complicated to make.

One option used by Cerebras is to use of redundancy to avoid having to bin devices that suffer major failures in one part of the die. Dividing arrays into smaller chiplets greatly increases the average yield in the face of random defects if redundancy is hard to implement.

At the International Solid State Circuits Conference (ISSCC) in February, AMD product technology architect Sam Naffziger said that assembling a 32-core Epyc processor from four chiplets instead putting everything on one die saved around 40 per cent in cost, even taking into account the redundant I/O logic each chiplet contained.

Another factor that points to the use of more, smaller chips is that lithography is moving in the wrong direction for monolithic silicon. The next generation of EUV scanners will use optical enhancement techniques that call for the area they can cover in one exposure to be halved. Chips with die sizes similar to nVidia's A100, which clocks in at 826sq mm, would need more than one pass for each mask.



Below: AMD's hypothetical Epyc 32-core processor could be assembled from four chiplets

What type of multichip integration?

The problem that faces chipmakers is deciding on what kind of multichip integration they should choose. The catalogue of multichip integration options from foundries and packaging houses keeps expanding. It started with CoWoS, which uses a large passive silicon interposer to support more than chip. Xilinx adopted it for larger members of the Virtex-7.

If the interconnect does not have to run underneath entire chips, another option is a silicon bridge. Altera, later acquired by the chip giant, used Intel's EMIB technology to provide short, low-capacitance links between the core programmable-logic array and I/O

chiplets for its larger FPGAs.

In the mobile market, fan-out wafer-level packaging (FOWLP), such as TSMC's InFO and ASE's FOCoS, are the options OEMs tend to pick. With the interconnect formed in an organic substrate, the cost is lower than for interposers, at the cost of fewer I/O lines.

Even within FOWLP, there are multiple choices for integration. The main option today is so-called chip-first where the silicon is embedded in the polymer and the circuitry formed around it. Chip-last is now appearing on some packaging menus to handle situations where the manufacturer wants to be sure the package works before inserting an expensive SoC into it.

Intel, TSMC and others are now looking to 3D stacking of devices. Though it's been a popular research topic for well over a decade, stacking has largely been confined to image sensors or package-on-package techniques where ultra-thin memories are combined in a single unit and integrated with the SoC using FOWLP.

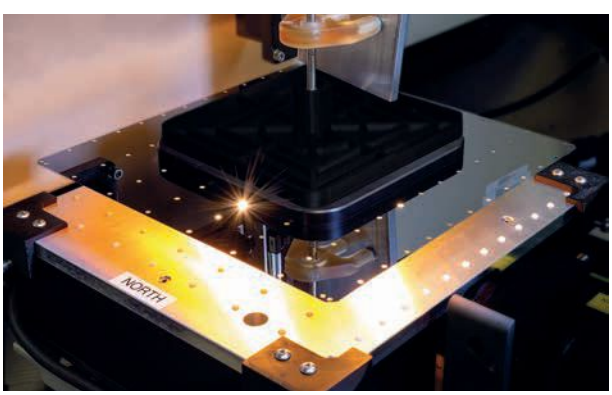
High-bandwidth memory (HBM) uses through-silicon vias (TSVs) to interconnect DRAM die in a single stack but has found it hard to gain traction because of its high cost. Again, the AI industry is turning to it, but primarily using side-by-side integration using interposers. That trend is leading to a growth in the size of the interposer.

At the company's symposium early this month, Jerry Tzou, director of the advanced packaging business at TSMC, said interposers that cover the area of two reticles are now ready and that a three-reticle option is likely to be qualified for production in 2022.

Thermal compatibility is a problem if DRAM is stacked directly on top of high-performance silicon. The hotspots need a higher refresh rate, which increases energy consumption and the need for cooling.

Instead, Badaroglu sees a brighter future for SRAM being stacked on top of processors for low-latency caches and working memory with DRAM used as bulk data memory mounted to the side. "We are seeing a significant trend on silicon interposer. With the larger area you pay more for the interposer but save on cooling cost," Badaroglu says.

Die-level yield and its effect on the final packaged yield remains the big issue for those looking to cut costs with disaggregation. The Microelectronics Packaging and Test Engineering Council has run a series of seminars on heterogeneous integration with one topic underlining the problem that manufacturers of multichip modules have faced for a long time. In one of those seminars last year, Jan Vardaman, founder and president of TechSearch International, asked rhetorically "after 30 years why are we still talking about known good die?". She pointed to a 1993 survey that identified the biggest barrier to multichip modules as being unable to identify defective unpackaged chips before assembly.



Below: Cerebras has developed a processing array that covers 50,000sq mm of silicon

Wafer-level testing

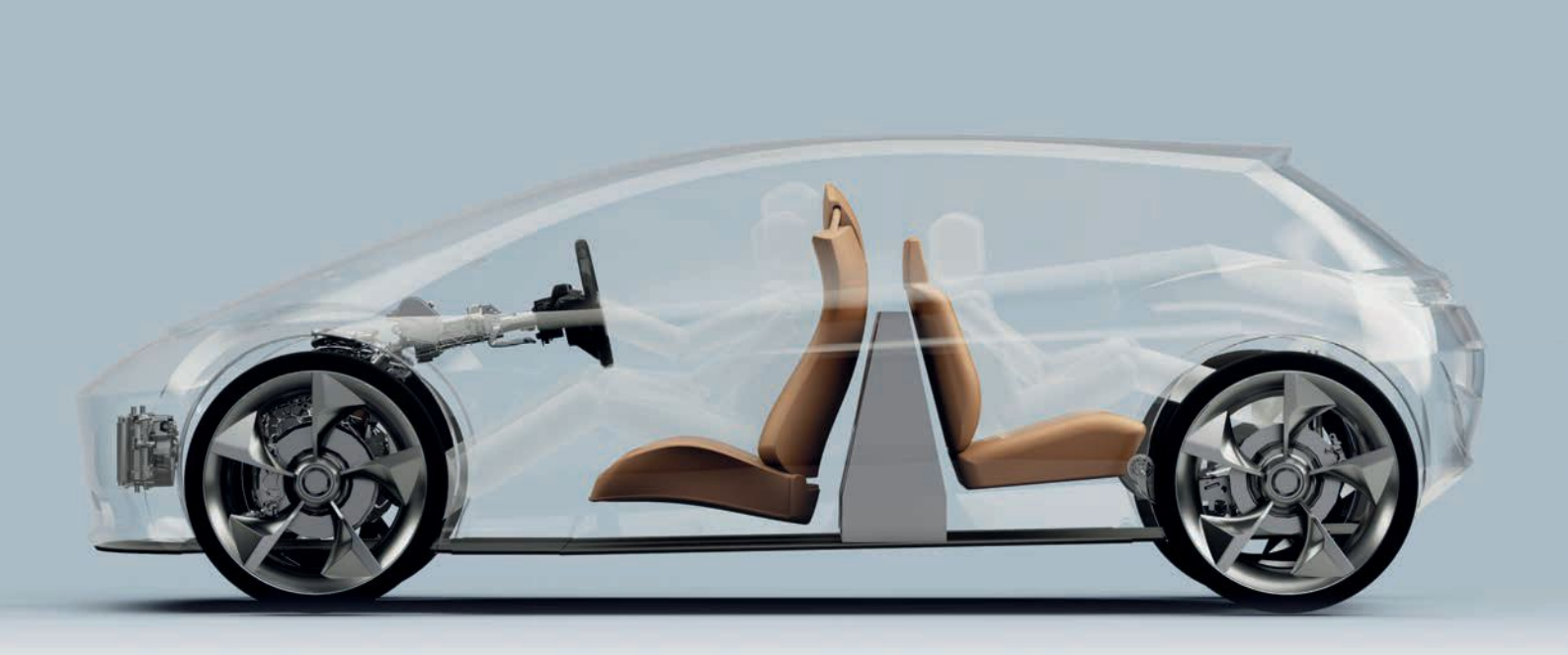
One way to deal with the doubt is improved wafer-level testing, though this has its own problems. The pads are so small that misalignment with a probe is inevitable. One response being pursued in proposed standards such as IEEE P1838 is to put more test logic into the chiplets so that they can test most of their connections and use the probe contacts to report their success or failure rather than rely on the contact measurements directly.

Built-in self-test coupled with redundancy will deal with many failures where the target device is a processor or memory array though there will inevitably be situations where redundancy cannot help.

Process management will likely come into play with machine learning being used to track how well certain wafers or batches fare in the field and to tune fab operations to minimise problems that keep turning up. Among others, the IRDS team is developing recommendations to minimise the kinds of contamination that cause random defects. Dan Wilcox, director of process engineering at Page Southerland Page, says the yield group is using test wafers with circuits created by the More Moore group to identify which contaminants are the most problematic.

The packaging process need not wait until the final chips are in place to start testing. AMD's recent work has involved progressively applying tests and measurements during assembly to weed out failures before they have committed too many expensive chips.

It is a learning process that has been going on for decades but which has suddenly accelerated and which, if successful, will provide an economically viable alternative to monolithic integration for a wider array of SoC projects.



NEW EV DESIGN CONCEPT

Start-up Page-Roberts has unveiled a patented design concept for an electric vehicle that's capable of travelling up to 30% further than current EVs. By **Neil Tyler**

Most electric vehicle (EV) designs see the car's battery placed under the floor and it's been a convenient way to package sufficient battery energy in order to develop an acceptable range.

There are, however, a number of drawbacks with this arrangement according to start-up Page-Roberts which has recently unveiled a new and patented design concept that looks to drive EV efficiencies by combining a 'cutting-edge engineering solution' with much greater design flexibility.

According to Page-Roberts CEO, Freddy Page-Roberts, "We have been looking to do something very different. While the skateboard arrangement found in current electric vehicles has become the mainstay this has resulted in taller vehicles with increased aerodynamic losses and energy consumption. There's also a need for extra structure to protect against impact and a longer wheelbase to account for the battery."

As a consequence the increased size and weight required has dramatically inhibited the range of current electric vehicles.

"Height, increased weight and the complexity of the vehicle's body structure have created these problems, but we have found that by simply moving the location of the battery pack we've been able to come up with a much more efficient solution," said Page-Roberts. "We believe that there is a real opportunity to build smaller and more efficient electric vehicles."

The challenges around electric vehicle design and roll-out focus on battery cost, energy density, range, the vehicle's weight and increasingly the lack of charging infrastructure – all of which are helping to stall progress in the EV category, despite an increasing number of leading brands and technology innovators racing to put their stamp on the market.

"The arrangement we've come up delivers a smaller, lighter and safer electric vehicle with a significantly enhanced range for an equivalent battery energy size," explained Page-Roberts, "and now we are in a position to talk to OEMs, investors and UK industrialists."

Lighter and more streamlined

The idea is to move the battery so that it's positioned between the front row seats and a second row of rear-facing seats delivering an arrangement that the company says is far more compact than standard electric vehicle designs and which offers the potential for a lower, more aerodynamic vehicle with a standard wheelbase.

"The resulting vehicle will be lighter and more streamlined, as a result," said Page-Roberts, "and it will offer the potential either for an extended range of up to 30% or the opportunity to use a much smaller battery to achieve a similar range. There are numerous new options for the configuration of the cabin which will make it suitable for a variety of vehicle configurations such as rear-facing seats, which are widely used in taxis and camper vans.

Above: By moving the battery Page-Roberts has come up with a more efficient vehicle design

"With increased design flexibility it will also be possible to improve outward visibility which, for many, is a key factor when it comes to enhancing and boosting occupant comfort. Their position ahead of the rear wheels will also provide enhanced passenger protection – such as reducing whiplash in the case of frontal impact," said Page-Roberts.

"There will need to be a discussion with OEMs as to the benefits of this arrangement but the concept of rear-facing seats is one that is increasingly popular when you look at ideas for autonomous vehicles, for example, but the key benefit is that it simply provides the opportunity to be more creative in terms of the cabin design."

According to the company the vehicle's lower weight will lead to what it describes as a 'virtuous circle'.

"A smaller battery, leads to lighter and lower cost motors, body, brakes and suspension systems," explained Page-Roberts.

Accordingly, the typical overall weight savings based on low-cost steel platforms could range from between 110 to 240 kg, while the torsion box arrangement from the battery pack lateral structure increases the structural efficiency of the vehicle, which in turn leads to further body structure weight saving opportunities.

"Weight is critical when it comes to electrical vehicles and this design is a lightweight solution that also delivers extended range, performance improvements, significant cost benefits and styling opportunities. Also by using new lightweight materials, solar panels and optimised propulsion systems it will be possible to further enhance those efficiencies," suggested Page-Roberts.

By using an under-floor battery another potential benefit is that newer, lower and sleeker designs will be possible that are capable of also reducing aerodynamic drag forces - the lower height enables greater rake to the vehicle surfaces, aiding aerodynamic efficiency.

"The aerodynamic drag forces can be typically reduced by as much as 20 to 30% compared with under-floor battery arrangements," said Page-Roberts.

By reducing the vehicle's weight and improving the aerodynamics typical efficiencies for this new arrangement based on standard components are said to be 130 to 180 Wh/mile based on WLTP and that's before taking into account the use of innovative technologies such as advanced aerodynamics or new lightweight materials that could help to deliver further additional benefits.

The Page-Roberts concept allows for large size batteries to be installed in smaller vehicles delivering much greater range when combined with the inherent efficiency of the arrangement.

"That can lead to requiring less time charging so the pressure on charging points – a major pain point for the industry – will also be reduced," added Page-Roberts.

The Page-Roberts design is particularly suited to small EVs, for which there is a very strong demand, despite most manufacturers focusing their attention on larger SUVs. The absence of batteries under the floor offers greater design freedom which, according to the company, could give rise to sleeker and sportier 4 seat vehicles.

"The average car journey in the UK includes just two people – so why do we continue building massive cars?" asked Page-Roberts. "Most people don't want overly large cars but, to be clear, our concept can address all vehicle sizes. We are looking at the battery arrangement pattern and that can be used in larger vehicles; at the moment we are geared to a smaller vehicle but there is real scope for this technology to be widely deployed.

"Smaller EVs are certainly better for urban environments and in our design, the rear-facing seats, whilst perfect for two additional passengers, also have the benefit of providing extra luggage space when not in use."

Below: Using an under-floor battery it will be possible to develop lower and sleeker vehicles

Manufacturing costs cut

When it comes to manufacturing, the company claims that costs can be cut by as much as 36% as a result of this unique battery arrangement.

"Our design avoids expensive aluminium or composite structures to compensate for the additional mass and poor structural complexity of the traditional skateboard platform used in most EVs. A 20% reduction in battery energy for a given range significantly reduces build cost and weight, while standardised lighter components lead to a virtuous circle of reduced complexity, weight and cost," said Page-Roberts.

These significant efficiency gains can also be translated into electric vehicles that have a far smaller carbon footprint – the ability to design vehicles with smaller batteries reduces the impact at the start of a vehicle's life and makes recycling the batteries easier.

According to Mark Simon, the company's CTO, "Our design concept reduces costs, increases efficiency, enhances agility, and offers design freedom. The efficiency translates to less time charging from either longer range or smaller batteries, so pressure on charging points will also be reduced."

"While these are significant efficiency gains they can also be translated into electric vehicles that have a far smaller carbon footprint.

"Rightfully, the environmental impact of producing and recycling batteries is a growing consideration for policy makers and manufacturers – the ability to design vehicles with smaller batteries reduces the impact at the start of a vehicle's life and makes recycling the batteries easier."

- **Launched in 2019, Page-Roberts bring together automotive pioneer Freddy Page-Roberts, and ex-Ricardo Project Director, Mark Simon. Both have extensive experience developing leading edge technology for automotive companies.**

One small step…

Stan Boland, CEO of Five, a leading UK self-driving start-up, talks about the challenges associated with delivering autonomous vehicles. By **Neil Tyler**

The hype around autonomous driving of a few years ago has given way to a growing realisation that when it comes to rolling out self-driving vehicles, it's going to be a lot more complex and challenging than many previously thought.

We're yet to see significant numbers of these vehicles on our roads and while the promises associated with the driverless revolution, whether making driving safer or delivering more environmentally friendly forms of transportation still ring true, it seems that engineers are beginning to realise that it will be a lot harder to deliver.

Stan Boland, CEO and co-founder of Five, has been leading the development of the company's self-driving systems since it was set up in 2015. Five has developed a cloud-based development and assurance platform which aims to help OEMs and other industry partners to accelerate the roll-out of autonomous systems.

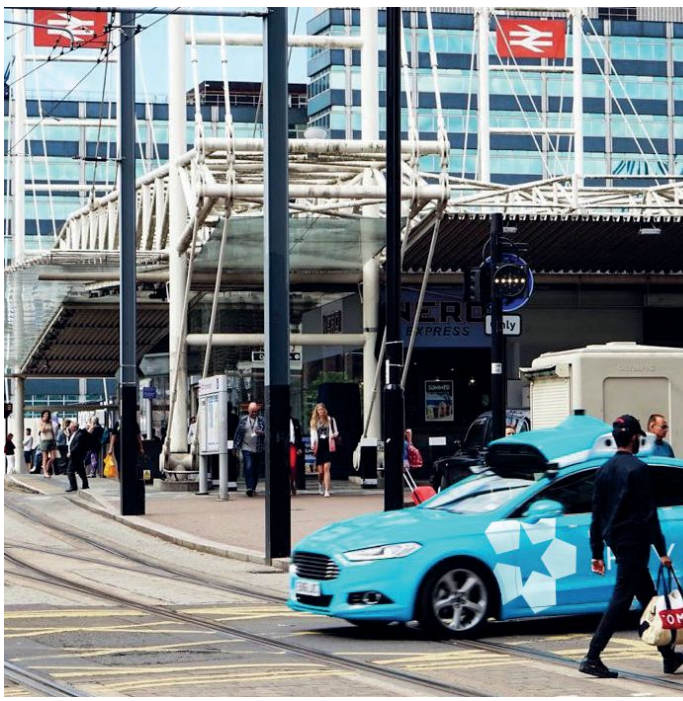
Back in 2019 Five led the UK government-backed Streetwise project to better understand the issues around the deployment of autonomous vehicles on UK roads. The company was heavily involved in the development of the complex software that was used to process the outputs from the cameras and on-board sensors that provided the data needed to predict and control the decisions made by the AVs. "The development of Automated Driving Systems (ADS) is possibly the greatest technological challenge of our time. The complexity is astonishing," admitted Boland, "and it's certainly more complex and challenging than many of us thought, especially when you are looking at operating an AV in an urban environment.

"When we set up Five our aim had been to build an autonomous driving system along the lines of Waymo, Uber ATG and Cruise. However, we soon realised that bringing this technology to market was going to be challenging and would require very deep pockets. As these systems have started to move from the proof of concept stage to operating in a functioning real-world environment it became obvious to us that there was still a long way to go before the technology would be widely deployed."

As a consequence, Five decided to 'pivot' from developing its own AVs to developing and focusing on the test and verification systems necessary to support their safe development.

"We realised from developing our own AV that how you went about demonstrating the safety of the system – which is by its very nature very complex – means you have to deal with thousands of potential interactions, each one of which can lead to serious error propagation. The urban environment in which we expect these vehicles to operate is extremely complex and there are no specifications telling you what to build, essentially you have to discover it for yourself and that requires an enormous amount of work."

It's the size, difficulty and expense of this challenge that is seen as a major factor in the hype around self-driving vehicles 'fizzling out' and it wont be until they've been effectively tackled that the widespread commercialisation of ADS technology will become a reality.



"To improve accuracy and reliability of perception it is necessary to fuse information from multiple sensors and detectors using an understanding of how likely to be correct the information will be."
Stan Bolan

Autonomous driving

At the heart of any autonomous system is the concept of 'Sense, Plan and Act' which defines the development of the autonomous vehicle. 'Sense' is about developing an internal model of the outside world, including the location of the ADS in that world; the 'Plan' is about developing a high level trajectory plan for the ADS based on goals, an interpretation of that model in the world and rules, and 'Act' translates that plan into acceptable forms of, for example, autonomous steering, acceleration, braking and signalling.

Sense is the component where 'AI' generally lives, often in the form of deep Convolutional Neural Networks (CNNs) interpreting LiDAR, radar and camera-based sensor outputs, while the Plan component lies within the traditional domain of robotics, although it is also required to plan under uncertainty, since the Sense component will never interpret the world completely accurately.

"The Streetwise project trialled one of our vehicles over mixed-use public roads in South London. The route complexity was high and our

software had to interact with a variety of real-world scenarios. The project offered a clear insight into technology readiness and passengers' reaction to it," explained Boland. "But it also highlighted the chasm that existed between a prototype project and a system that is able to detect, understand, predict and plan at all times reliably in a complex real world situation."

While Five demonstrated that its reference ADS could operate at high safety even on public roads, making over 100 public test drives in a single month across a complex 21km route in South London, it learned a great deal about the types of errors that could arise and impact the decision-making of the system.

"When it comes to perception errors they are critical and will have a profound impact in planning errors. When entering a roundabout if the system isn't seeing the road or orientation of vehicles correctly – it could be off by a matter of a few degrees or centimetres – then the ride will not be smooth or safe."

According to Boland too much testing and verification is done in isolation and what was needed was an end-to-end solution that brought perception and planning together.

"To improve accuracy and reliability of perception it is necessary to fuse information from multiple sensors and detectors using an understanding of how likely to be correct the information will be. Also, we believe it is impossible to label sufficient data to solve or verify or validate these real world problems, so it is also essential to find techniques able to make use of unlabelled data

"You can't test these vehicles for every conceivable scenario. That would require you driving a test vehicle upwards of 8.8bn miles, so you have to turn to the virtual world," added Boland.

"When we started building a completely new self-driving system it required Five to create a cloud-based platform to help develop and test the technology and we came to realise that platforms like this would be essential to unlocking the full potential of self-driving systems.

"We're now rolling out our platform to industry partners to help them build better self-driving systems, shortening their time to market, and enabling the delivery of evidence-based safety arguments."

Five's platform is highly sophisticated and provides specific development tools that are able to measure and deliver safety assurance for the whole autonomous system.

"You're able to choose or create your own scenario, run varied simulations, then evaluate them and based on that refine your stack. A cloud based system makes it possible to explore different scenarios more quickly and to identify faults by exploring the most relevant scenarios."

Left: Five led the UK government backed Streetwise project in 2019

Boland said that too many of the existing measures for safety performance were too simplistic and inefficient and actually hid many of the system's failures, which in turn slowed down the development process.

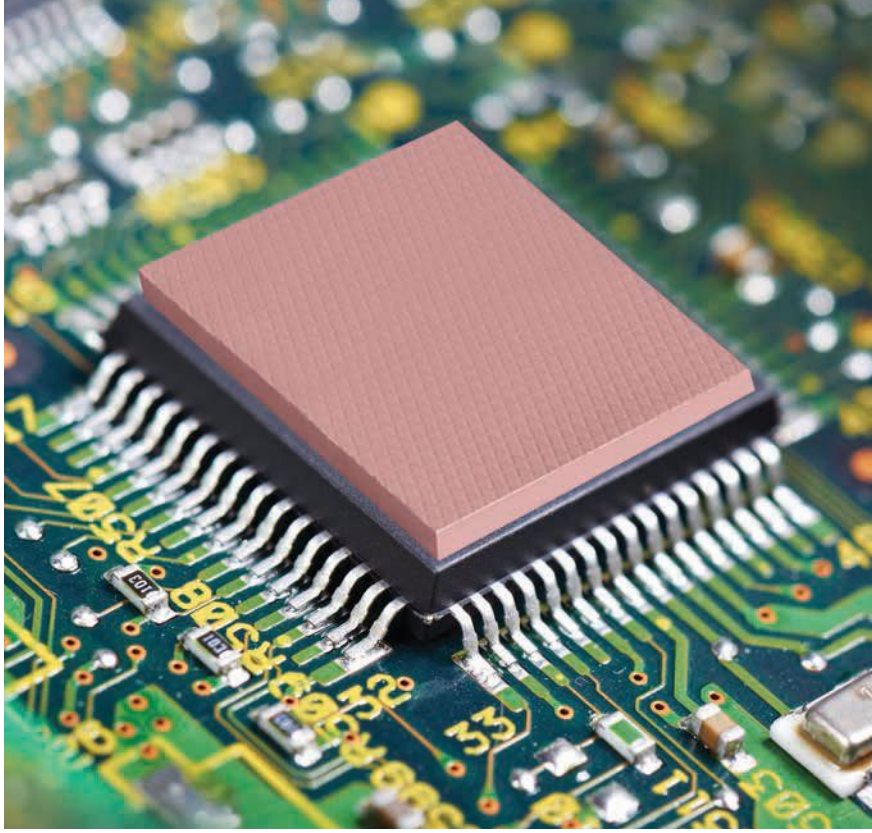
"As a result there was a need for a more efficient and powerful form of simulation, capable of creating more experiences for the system than taking a vehicle for an actual ride."

Collaborative efforts such as StreetWise showed that bringing self-driving to fruition will be a team effort with partners working together to solve complex multi-disciplinary issues and while Five's development of its platform has gathered pace – it's now being used in other projects to speed up developments and improve safety assurance – the successful roll-out of autonomous vehicles will require companies to work differently and to collaborate more.

"We are seeing the development of a whole new AV ecosystem in what is a very broad field – from software to sensors and the application of neural networks. To be successful the big players in this space will need to successfully orchestrate a complex network of suppliers. It's coming together but the challenges around AVs remain significant."

Examining whether to **GEL** or **PAD**

New electronic product generations bring with them new challenges concerning thermal management, as **Jonathan Appert** explains



Above: A therma gap pad chip

New electronic product generations bring new challenges associated with thermal management and while there are two general types of thermal interface materials: gels (or dispensable gap fillers) and gap filler pads, both of which displace air voids and ensure proper heat transfer, each one has distinct advantages depending on the application.

Demand for effective thermal interface materials is rising in direct response to changing needs in the electronics packaging market.

The objective of thermal management in electronics packaging is the efficient removal of heat from the semiconductor junction to the ambient environment and this process can be separated into three phases:

1 Heat transfer within the semiconductor component package
2 Heat transfer from the package to a heat dissipater (the initial heat sink)
3 Heat transfer from the heat dissipater to the ambient environment (the ultimate heat sink)

The first phase is generally beyond the control of system-level thermal engineers because the package type defines the internal heat-transfer processes. In the second and third phases, the packaging engineer's goal is to design an efficient thermal connection from the package surface to the initial heat spreader and on to the ambient environment.

Achieving this ambition requires a thorough understanding of heat-transfer fundamentals, as well as knowledge of available interface materials and their key physical properties.

When evaluating thermal interface materials, engineers look to identify high-performance products that meet the thermal, design, manufacturing and cost challenges inherent in each customised application.

Gap filler pads and gels

Both pads and gels offer effective means of thermal management. While pads have a longer proven track record, recent advances in gels have, in some cases, surpassed their performance. The following are ways that newly engineered gels compare with gap pads in matters of critical importance to design engineers.

Both gels and pads are conformable to a degree, but the maximum configurability of a gap pad is less than that of a gel due to its solid structure.

Flow rate

The goal when developing gels is to achieve the highest and most repeatable flow rate. Customers want to set their dispensing equipment for the same flow rate batch-to-batch to maintain a consistent volume and avoid wasting any material. Newer gel technologies achieve a more repeatable and higher flow rate that improves throughput and reduces waste.

Identifying the amount of heat (Watts) in need of dissipation will determine the thermal conductivity performance required of the application's gap filler. The higher the value, the more heat the material can theoretically dissipate. Industry-wide, the thermal conductivity of gap pads and gels can range from 1 to 10 W/m-K (Watts per meter Kelvin).

While this issue might be the great unknown in real-world applications because of the newness of advanced gels, rigorous accelerated aging tests can be used to aid long-term reliability. Three different aging treatments can be performed on a fixture with the gel compressed between two stainless steel panels: a dry heat soak at 125° C; heat and humidity at 85° C and 85% relative humidity; and temperature cycling from -40° to 125° C. Future state, a thermal shock element is added, while vibration testing is also performed based on the GMW3172 standard.

In the curing process, cross-linking refers to relatively small molecules joining much larger polymer chains in the thermal interface material.

Although both pads and gels cure via the same cross-linking mechanism, in a pad there are more cross-links, which leads to a stronger cure. Curing contributes to the viscoelastic properties of gels, which improves their form stability over a non-cured system.

Assembly and cost dynamics

The opportunity for automation is a significant advantage when it comes to gels. While pad placement can be automated to some extent, the equipment and fixtures required is typically specialized and may not readily adapt from one job to another.

Production speed will be application-dependent, but to illustrate the potential advantage of gels, consider a specific customer example. This particular customer was contemplating a switch from pads to gels and tested both materials to gauge the difference in throughput. The study revealed that it took an operator 18 seconds to apply one pad manually, but this process reduced to just four seconds using a gel and an automated process.

The argument favouring gels grows even more convincing if there are multiple dispense locations on a single part. An automated/robotic gel dispenser can hit each location in one cycle, contrasting greatly to the manual, individual application of gap pads.

When placing a gap pad, the operator needs to know its orientation. There is a top side and bottom side, and in many instances, there are left-right and/or up-down orientations. Whereas manual pad application introduces more risk of human error, with gel application the metered gel is simply dispensed onto a specific location.

Precision and shape

One benefit of gap pads is that they can be cut to the exact shape of the customer's part, whereas gel adopts its post-compression shape. The specific application will drive the degree of precision required, as well as determine the acceptability of gel expansion beyond the application surface.

The choice of gel shape can help determine and control the ease of application and any resulting spread. For instance, a dot shape is the easiest to dispense and will result in a roundish cross-section. An X-shape or serpentine pattern results in a square cross-section at the expense of throughput. Very complex or thin shapes may not necessarily be well accommodated with die-cut gap pads; a gel may be able to achieve those geometries better.

To maximize thermal performance, the interface material must contact the entire target area on both the component and heat-sink surfaces without air entrapment. A simple dot pattern provides adequate coverage, the shortest cycle time and the least chance of introducing air into the thermal interface material. The more complex the profile is, so the greater the probability for introducing air (e.g., serpentine and spiral).

Broadly speaking, gels tend to be less expensive on a volume basis against comparable gap pads. Experience with multiple applications suggests that about 5,000 parts per year is the threshold where it becomes more economical to use gels and an automated dispensing system versus manual pad application (depending on shape and geometry).

Dispensing equipment investment can start at $10,000 to $30,000 for low-volume table-top units that require an operator. Increased sophistication and added features like camera recognition for quality control bring the equipment cost to $80,000 to $120,000, plus installation and training.

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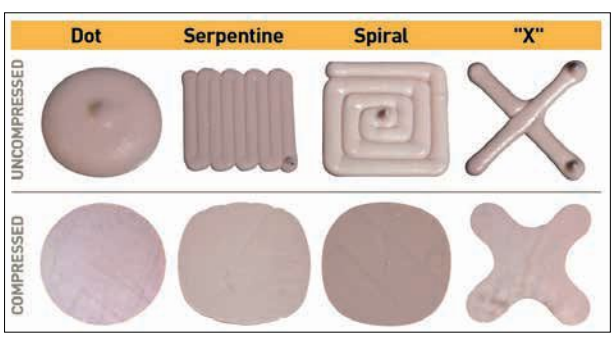


Below: Gels vs Pads - dispensing patterns compared

Packaging solutions

Gel packaging starts in 10 cc cartridges, which are suitable for use as samples, or for manual low-volume applications. The next tier up is a variety of pneumatic-dispensed cartridges ranging from 30 to 600 cc. These cartridges require simple dispensing equipment, such as a high-pressure air line with a regulator and nozzle. An operator can dispense manually or there could be some type of robot-assist mechanism. The largest packages, supporting the highest throughput volumes, are one- or five-gallon pails, which require a pneumatic pump to push the material into a secondary metering valve.

While a geometrically complex die-cut part pad has costs associated with development and production, there are other options if a customer has a lower budget and wants to handle pad cutting in-house. For instance, pads are available in sheet form that can be readily cut or trimmed prior to application. In terms of gel dispensing, the provision of more control allows customers to make changes on the fly without having to modify a drawing, perform a first-article inspection, or complete formal engineering change procedures.

Gap filler pads have long been the go-to choice for many design engineers. However, recent advances means that thermal gels can provide superior performance, easier manufacturing and assembly, and a lower cost in certain high-volume applications; particularly as electronic design applications get smaller, more fragile and more complex. Ultimately, maintaining an open mind to using the latest gels is a consideration that could pay off in performance, manufacturing efficiency and cost savings.

Capitalising on the **mmWave** spectrum

Advanced circulators are being used to overcome serious mmWave design challenges, as New Electronics discovers

Greater isolation and bandwidth will enable telecom providers and radar technology designers to be able to fully capitalise on the mmWave spectrum.

As communications providers race to deliver on the potential of 5G, research and design projects are already looking towards 6G and beyond. The promise of ultra-fast broadband speeds – potentially as much as 10 Gbit/s – are seen as helping to catapult cellular technology into new markets like smart cities, connected vehicles, defence, and the rapidly expanding IoT. However, a major hurdle awaits the impending move up the millimeter wave (mmWave) spectrum; that being a lack of acceptable mmWave components such as circulators.

"It is an enormous technical challenge we are facing," explained Fred Daneshgaran, a California State University, Los Angeles, professor who specialises in RF design, telecommunications and quantum communications. As such, Daneshgaran is frequently brought in as lead technician on some of the most cutting-edge RF military and telecom projects.

"The only way to support the billions of users at higher data rates is to keep utilising higher and higher frequency bands, so components are going to have to catch up," said Daneshgaran. "The problem is, however, as you go up the spectrum it gets harder and harder to build critical components like circulators that can operate at those frequencies."

Moving on up

The higher-end of the 5G spectrum (26GHz to 86GHz) will provide much of the leap forward in data speeds, capacity, quality and reduced latency. However, at such frequencies the design of transmit/receive components becomes critical. Without advancements, the deployment of systems capable of operating even higher on the spectrum - within the terahertz regime (100 GHz – 10 THz) where 6G and 7G will operate - are also in jeopardy.

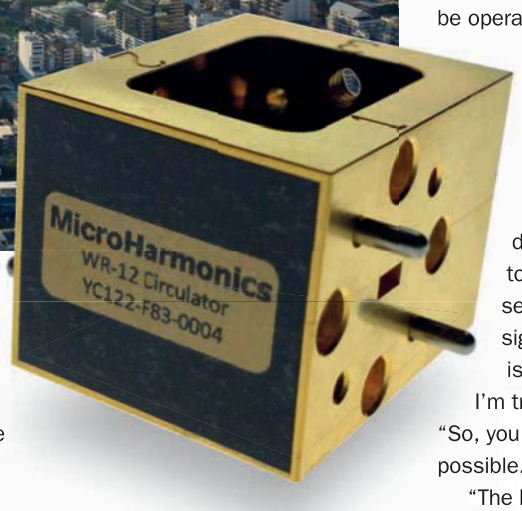
Recognising that national security could be affected, towards the end of last year, the US Department of Defense announced $600 million in awards for 5G experimentation and testing. Given this impetus, microwave components such as antennas, waveguides, isolators and circulators are now being developed that are capable of broadband operation at mmWave frequencies up to 330GHz and beyond.

"One component that is especially critical to telecom infrastructure is the circulator," Daneshgaran explained. "Antenna systems capable of both transmitting and receiving a signal are typically expensive because they are reciprocal devices. To keep the signals separated you have to put something like a circulator at the front end, otherwise you'd need two different antennas."

Basically, a circulator is a three-port device in which power entering any port is transmitted to the next port in rotation. As a result, any signal that goes into port one, goes out port two, and any signal coming in port two, goes out to port three.

This issue of duplexing at mmWave frequencies is not only problematic for telecom applications, but also for radar technology which

relies on circulators to separate the signal on the transmission path from the signal on the receiving side.



Above: Circulators are critical components in keeping signals separated

Overcoming performance challenges

In a recent effort to design and build an R&D system for a major commercial contractor, the lack of a circulator capable of operating at 120GHz stopped Daneshgaran's team in its tracks.

"Theoretically, you can design one, then simulate its performance, and it will be fine. However, actually making them is more of an art than a science," explained Daneshgaran. "It is just very hard to build circulators at the mmWave range."

"At first, we couldn't find anybody that was capable of producing circulators in the frequency band we required, much less with the high isolation and wide bandwidth we wanted," added Daneshgaran.

In a continued search for a circulator with the necessary attributes, Daneshgaran and his team approached Micro Harmonics, who had developed a circulator for mmWave systems while working with NASA on a number of SBIR projects.

Micro Harmonics specialises in components designed specifically for mmWave applications and has successfully developed an advanced line of circulators operating from 25GHz up to 150GHz.

"Micro Harmonics fine-tuned the design to meet the performance characteristics we needed within the very precise band we were going to be operating on," said Daneshgaran.

Whether it's for high-speed data transmission and reception, or for target detection, isolation is a key parameter.

"If the circulator doesn't have good port-to-port isolation, you get self-interference; meaning the signal I'm trying to transmit is interfering with the signal I'm trying to receive," he added. "So, you want as much isolation as possible."

"The Micro Harmonics circulators demonstrated some pretty impressive isolations," continued Daneshgaran. "At the frequency we operated on, we realised almost 30 dB of port-to-port isolation, which is a lot. Typically, it is very hard to even get above 20."

A circulator must also offer a wide bandwidth, a major challenge at mmWave frequencies.

"For telecoms, the more bandwidth you have the more data you can support," said Daneshgaran. "This is because your data rate is directly proportional to the amount of bandwidth you have around your carrier frequency."

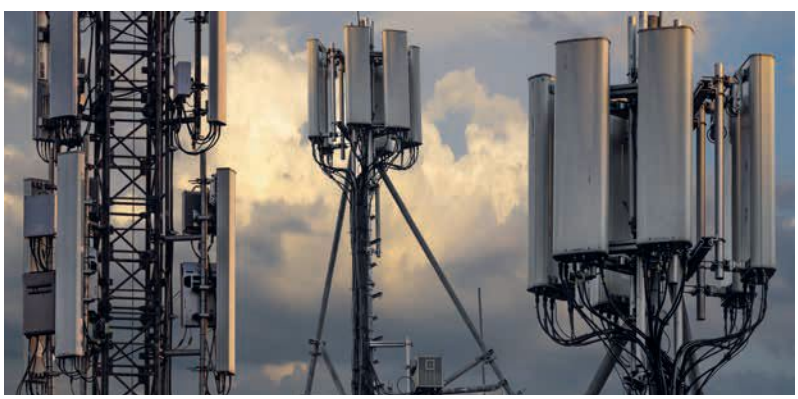
Daneshgaran goes on to explain that in a radar application, wide bandwidth is important because it involves continuous frequency sweeps. The larger the bandwidth, the easier it is to discern a target in a given sweep.

In Micro Harmonics' case, increased bandwidth for its circulators is achieved by abandoning complicated dielectric impedance-matching elements in favour of a mechanical engineering solution. This makes the performance highly repeatable from one assembly to the next.

"With these circulators we are getting a clean 'couple of gigahertz,' if not more, of bandwidth within the characteristic limits of 30 dB isolation we seek for our application," noted Daneshgaran. "If we were willing to accept something like 20 dB of port isolation, we could have four or more gigahertz of bandwidth, which is very significant."

"Because of the initial delays in finding workable mmWave components, we really needed to jump in and make several measurements that we had fallen behind on," concluded Daneshgaran.

"With the implementation of advanced circulators our machine has been running continuously ever since we set it up, and the results we have achieved have been very impressive."



Left: A lack of acceptable components could hinder the use of the mmWave spectrum

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Demystifying medical alarm designs

Using smart DACs can help in the design of complex medical alarms, as a team from Texas Instruments explains to New Electronics

Author details:
Uttama Kumar Sahu and Snajay Pithadia are System Engineers and Ivan Salazar an Applications Engineer, from Texas Instruments

Medical alarm designs require expertise in hardware, software, acoustics as well as an in-depth understanding of the regulatory requirements. The DAC53701 smart DAC, from Texas Instruments, provides a far simpler way to implement the alarm with configurable in-built waveforms triggered by a GPI.

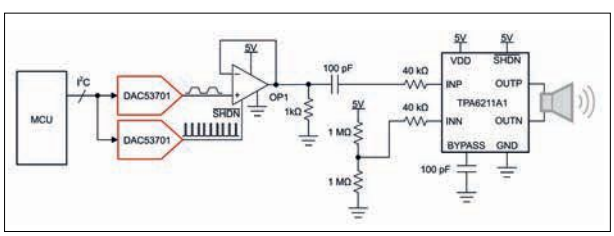
Medical alarms are a critical part of most medical devices used in intensive care units (ICU), such as multi-parameter patient monitors, neonatal warmers and incubators, anaesthesia delivery systems, dialysis machines, infusion pumps, ventilators, and surgical equipment.

A patient's health and well-being often depend on the proper functionality of medical devices and medical alarms play an important role in alerting the caregiver when a failure event occurs.

All medical devices need single-fault protection. A single-fault condition in medical equipment refers to the presence of a single independent abnormal condition. During a single-fault condition, a medical device must provide basic safety from physical hazards and minimum functionality, known as essential performance.

While basic safety is usually obtained through isolation and leakage control, the alarm function is a key contributor to the essential performance for most therapeutic and all critical-care medical devices. The DAC53701 smart DAC provides integrated medical alarm functions compatible with the IEC60601-1-8 standard, such as different alarm priorities, pulse frequency, and burst patterns with configurable timings, thus simplifying the design and shortening the development time.

Figure 1: Primary auditory alarm



Smart DAC - DAC53701

The device is a 10-bit smart digital-to analogue converter (DAC) with non-volatile memory (NVM), I2C interface, and general-purpose input (GPI). This device is available in a tiny, 2-mm x 2-mm package and it is able to support medical alarm generation using pre-programmed waveforms. The waveforms can be triggered by both I2C and GPI interfaces. This DAC can be used for both auditory and visual alarm generation and it supports configurability of the pulse frequency and the timings for the pulse envelope and the burst.

Primary auditory alarm

For the primary auditory alarm implementation, two DAC53701 devices are required: one device is used to generate the pulse envelope and the burst, and the second to generate the pulse frequency as shown in Figure 1.

The signals coming from both the DACs are combined together using the amplifier OP1 that has a shutdown pin, for example, the TLV9002S or OPA363 devices. The combined signal is then ACcoupled to an audio amplifier, such as the TPA6211A1, to drive the speaker.

The TPA6211A1 is an integrated Class-AB amplifier which can drive up to 3 W of output power with very little distortion. The waveforms at different nodes of the circuit in Figure 1 are shown in Figure 2.

As per the IEC60601-1-8 medical alarm standard, the pulse frequency must be above 150 Hz and must have at least four harmonic components that are within ±15 dB of each other. As a result of the square wave pulse frequency and the mixing done by OP1, the speaker output generates multiple harmonics of the fundamental pulse frequency.

The DAC53701 provides a range of timing options for the pulse frequency and the pulse envelope.

Visual alarm

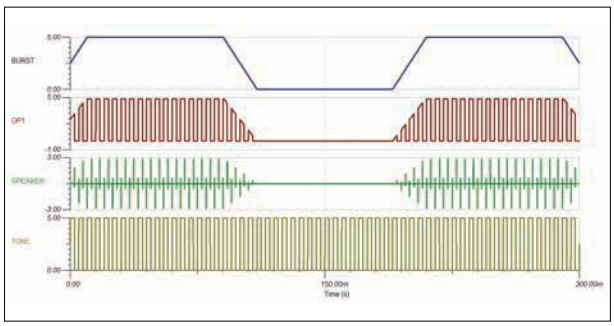
The output of the DAC53701 can also be used to drive the visual alarm LEDs as shown in Figure 3. For redundancy, it is recommended that another DAC53701 device is used and does not share the DAC from the auditory alarm.

The force sense output of the DAC53701 helps drive the gate and source of the MOSFET directly and, as a result, compensates for the drift of the gate-to-source voltage (VGS). The circuit in Figure 3 provides linear control of the LED.

In case high-power LEDs are used, a switching LED driver is preferred to linear control for power efficiency and the DAC output can drive the current control pin of the LED driver.

Secondary alarm

The medical alarm is part of the essential performance for most medical devices. Hence, it is responsible to alert the caregiver in case of any failure event that does not have any redundant protection mechanisms.



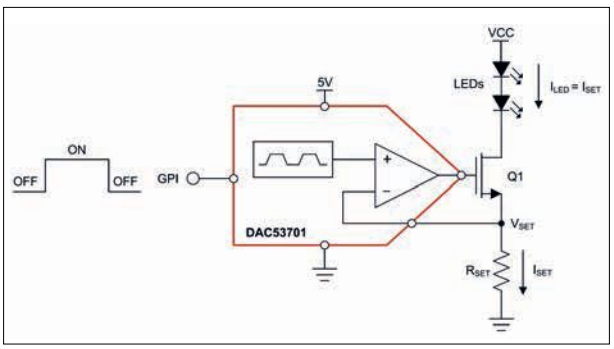


Figure 2: Auditory alarm waveforms

Figure 3: Visual alarm

A power failure for mains-powered medical devices or battery discharge for battery-powered medical devices can be fatal to the patient. A similar risk may also occur in case of the failure of the primary alarm system. As a consequence, an independent alarm is used to indicate power failure or the failure of the primary alarm system. This secondary alarm is usually triggered by a secondary processor, a watchdog timer, or a power failure detection circuit.

This alarm circuit is typically powered by a supercapacitor or a battery. Particular medical device standards specify a minimum ON-time for the power failure alarm. Simplistic implementations of secondary alarms often connect an internally driven buzzer to a supercapacitor directly. Such implementations generate a single tone alarm that is hard to modify.

Figure 4 shows a circuit for creating a more effective alarm implementation where custom patterns can be generated using a single or two DAC53701 devices and inexpensive externally driven transducers. Custom alarm patterns help distinguish the alarm more clearly in a crowded ICU setup as compared to a single tone. The DAC53701 operates at very low quiescent current thus increasing the duration of the power failure alarm running from a supercapacitor.

Volume control

Medical devices need volume control for the alarms and the DAC53701 provides 3 gain control settings that can be used for volume control. A more granular control can also be achieved by controlling the maximum level of the alarm waveforms through the margin-high register bits.

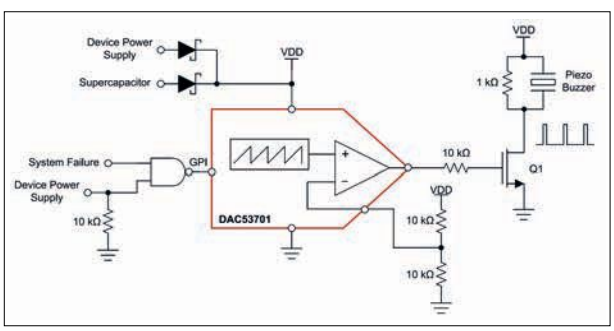
Conclusion

Creating designs for medical alarms can be challenging due to complex regulatory requirements, multi-domain expertise requirements, tuning requirements during testing, portability of the design across multiple end equipment, and total time and cost of the development.

Conventional techniques tend to lack in providing a holistic solution, however, the DAC53701 provides a simple way to create medical alarm designs by addressing all the technical and non-technical challenges.

This device can be used for both primary and secondary or auditory and visual alarm implementations and the tiny package also makes the solution suitable for small form factor designs.

Figure 4. Secondary alarm



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Lattice sensAI Solution Stack Simplifies Deployment of AI/ML Models on Smart Edge Devices

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Supports TensorFlow Lite and Lattice Propel for Embedded Processor-based Designs; Includes New Lattice sensAI Studio Tool for Easy ML Model Training

Lattice Semiconductor Corporation (NASDAQ: LSCC), the low power programmable leader, today announced enhancements to its award-winning Lattice sensAI™ solution stack for accelerating AI/ML application development on low power Lattice FPGAs. Enhancements include support for the Lattice Propel™ design environment for embedded processor-based development and the TensorFlow Lite deep-learning framework for on-device inferencing. The new version includes the Lattice sensAI Studio design environment for end-to-end ML model training, validation, and compilation. With sensAI 4.0, developers can use a simple drag-and-drop interface to build FPGA designs with a RISC-V processor and a CNN acceleration engine to enable the quick and easy implementation of ML applications on power-constrained Edge devices.

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New HV SPDT Form C reed relays from Pickering save space and design complexity

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Compact Series 67 1 Form C relays rated up to 5kV

Pickering Electronics, the reed relay company which has pioneered miniaturization and high performance for over 50 years, has introduced a new changeover 1 Form C version of its popular Series 67 high voltage PCB relay that saves space and makes design simple.

Explains Kevin Mallett, Technical Specialist at Pickering Electronics: "In applications where high voltage signals need to be routed to alternate points, polarity reversing, capacitor charge or discharge for example, a high voltage Changeover relay (SPDT/Form C) would be the ideal solution. These are often implemented using two Normally Open (SPST/Form A) high voltage relays, by ensuring that one switch is always opened before the second switch is closed. This requires twice the PCB area and can cause complex driving issues. Also, if either of the SPST relays sticks then there is risk of unintentionally shorting signals." Pickering's new 67-1-C high voltage reed relay guarantees break-before-make operation in a single, compact part.

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Nicomatic's 1mm pitch AMM Series now available in days – saves space and weight

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Five standard layouts available on 3 – 5 day lead time; highly modular series with multiple configurations to order; MOQ 1

Nicomatic, the leading manufacturer of high performance interconnect systems, announces that its 1mm pitch AMM Series is now available in five standard layouts for delivery on only a few days' lead time. The AMM Series saves both space and weight in the most demanding aerospace and other hi-rel applications, including medical, defence & security and harsh-environment industrial.

The five standard layouts available within 3 – 5 days are 6, 10, 20, 34 and 50 contact interconnects with 2 rows. Featuring an integrated guidance pin for ease of stacking, these AMM Series connectors are available for thru-mount on PCBs or straight surface PCB mounting (AMM A22 Series, male and female versions) and pre-wired (AMM HA22 Series, female).

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211 new PXIe modules launched. Visit Pickering on booth 1841 at the International Microwave Symposium, June 8-9 Atlanta, GA., USA (In-Person Event); and June 20-25 (Virtual Event)

Pickering Interfaces, the leading supplier of modular signal switching and simulation solutions for electronic test and verification, announced that it now offers all its RF & Microwave PXI products that operate at 3GHz or above in optional PXIe format. This includes the recently released 40/42-785C (PXI / PXIe) range of microwave multiplexers that offer a maximum frequency of 67GHz in both SP4T and SP6T form factors.

Pickering has a continuous R&D program, introducing many new and innovative products each year, and now offers a catalog of over 1,000 PXI products. The most recent designs are being released simultaneously in both PXI and PXIe formats. Because the software and hardware functionality between PXI and PXIe versions is identical, the company has already been able to port several hundred of its current PXI modules to the PXIe format, now including 211 RF & Microwave modules.

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Power Integrations Introduces InnoSwitch4-CZ Flyback Switcher ICs

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Anker selects zero voltage switching InnoSwitch4-CZ ICs with PowiGaN technology for new ultra-compact 30, 45 & 65 W USB-C Nano II charger series

Power Integrations (Nasdaq: POWI), the leader in high-voltage integrated circuits for energy-efficient power conversion, today announced the InnoSwitch™4-CZ family of high frequency, zero voltage switching (ZVS) flyback switcher ICs. InnoSwitch4-CZ devices incorporate a robust 750 V primary switch using Power Integrations' PowiGaN™ technology and a novel high frequency active clamp flyback controller to facilitate a new class of ultra-compact chargers suitable for phones, tablets, and laptops. The first consumer devices based on InnoSwitch4-CZ devices were introduced by Anker, the global charging experts for mobile devices.

Balu Balakrishnan, CEO of Power Integrations said: "The introduction of the InnoSwitch4-CZ family of ICs marks a significant milestone for GaN technology. PowiGaN switches, in conjunction with our active clamp solution – ClampZero™, enable a highly efficient design and an extremely compact form-factor. We're pleased to have worked closely with the Anker team to bring this new class of mobile charger to market."

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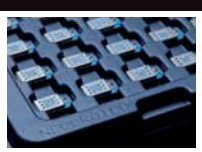

NeoCortec, manufacturer of the world's smallest, ultra-low-power bi-directional wireless mesh network modules, has signed a global distribution agreement with Mouser Electronics, the leading New Product Introduction (NPI) distributor. Mouser will stock NeoCortec's range of wireless connectivity devices, including NC1000 and NC2400 network modules, Mini PCI Express (PCIe) interface modules and breakout boards. Headquartered in Copenhagen, Denmark, NeoCortec develops mesh technologies and solutions for wireless sensor networks, enabling large-scale routing networks to operate in real time while simultaneously reducing power consumption. The unique NeoCortec protocol stack is offered for both 2.4GHz as well as sub 1GHz frequency bands, delivered in a series of pre-approved modules. Cost efficient and easy to integrate, the modules suit a broad range of applications based on IoT and Cloud-based sensor networks, including smart home and smart workplace, metering, security, agriculture, transportation, industry 4.0, medical and food distribution. All NeoCortec modules share the same tiny 11x18x2.6mm footprint, so the target product does not need to change to support a full range of frequency bands. Average power consumption is as low as 20A

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